CLAIMS

What is claimed is:

1. A bias generator for cell self refresh, comprising:

   a. a first current generator adapted to generate a first leakage current for "0" state cells;

   b. a second current generator adapted to generate a second leakage current for "1" state cells; and

   c. a converter coupled to the first and second current generators, the converter adapted to transform a current comprising the first leakage current and the second leakage current into an output bias.

2. The bias generator of claim 1 further comprising a third current generator coupled to the converter, the third current generator adapted to generate a third current and provide the third current to the converter.

3. The bias generator of claim 1, wherein the first current generator comprises:

   a. a "0" state cell, further comprising a storage node; and

   b. a first current mirror circuit coupled to the storage node.

4. The bias generator of claim 3, wherein the first current mirror circuit further comprises:

a. a first metal-oxide-semiconductor (MOS) transistor coupled to the storage node; and

b. a second MOS transistor coupled to the converter.

5. The bias generator of claim 4, wherein the first and second MOS transistors are NMOS transistors.

6. The bias generator of claim 5, wherein the first current mirror circuit is further adapted to generate a current weighting factor utilizing a ratio of a physical characteristic of the first NMOS transistor and a physical characteristic of the second NMOS transistor.

7. The bias generator of claim 1, wherein the second current generator further comprises:

a. a "1" state cell, further comprising a storage node; and

b. a second current mirror circuit coupled to the storage node.

8. The bias generator of claim 7, wherein the second current mirror circuit further comprises:

a. a first MOS transistor coupled to the storage node; and

b. a second MOS transistor coupled to the converter.

9. The bias generator of claim 8, wherein the first and second MOS transistors of the second current mirror circuit are PMOS transistors.

10. The bias generator of claim 9, wherein the second mirror circuit is adapted to generate a current weighting factor utilizing a ratio a physical characteristic of the first PMOS transistor and a physical characteristic of the second PMOS transistor.

11. The bias generator of claim 1, wherein the converter further comprises:

a. a third current mirror circuit; and

b. a common gate transistor.

12. The bias generator of claim 11, wherein the third current mirror circuit comprises a pair of same type MOS transistors.

13. The bias generator of claim 1, wherein the output bias comprises at least one of (i) an NBias or (ii) a PBias.

14. A circuit for generating a periodic pulse signal for cell self refresh, comprising:

a. a bias generator adapted to accumulate a leakage current generated from a memory cell and further adapted to generate an output bias useful for determining a self refresh period; and

b. an oscillator adapted to generate a periodical signal pulse in response to the output bias.

15. The circuit of claim 14 wherein the bias generator further comprises:

a. a first current generator adapted to generate a first leakage current for a "0" state cell;

b. a second current generator adapted to generate a second leakage current for a "1" state cell; and

c. a converter coupled to the first and second current generators, the converter adapted to transform a current comprising the first leakage current and the second leakage current into the output bias.

16. The circuit of claim 15 further comprising a third current generator, coupled to the converter and adapted to generate a third leakage current and provide the third leakabe current to the converter.

17. The circuit of claim 15, wherein the first current generator further comprises:

a. a "0" state cell, further comprising a storage node; and

b. a first current mirror circuit coupled to the storage node.

18. The circuit of claim 17, wherein the first current mirror circuit further comprises:

a. a first metal-oxide-semiconductor (MOS) transistor coupled to the storage node; and

b. a second MOS transistor coupled to the converter.

19. The circuit of claim 18, wherein the first and second MOS transistors are NMOS transistors.

20. The circuit of claim 18, wherein the first current mirror circuit is adapted to generate a current weighting factor utilizing a ratio of a physical characteristic of the first NMOS transistor to a physical characteristic of the second NMOS transistor.

21. The circuit of claim 15, wherein the second current generator comprises:

a. a "1" state cell, further comprising a storage node; and

b. a second current mirror circuit coupled to the storage node.

22. The circuit of claim 21, wherein the second current mirror circuit further comprises:

a. a first MOS transistor coupled to the storage node; and

b. a second MOS transistor coupled to the converter.

23. The circuit of claim 22, wherein the first and second MOS transistors are PMOS transistors.

24. The circuit of claim 23, wherein the second mirror circuit is adapted to generate a current weighting factor utilizing a ratio of a physical characteristic of the first PMOS transistor to a physical characteristic of the second PMOS transistor.

25. The circuit of claim 15, wherein the converter further comprises:

a. a third current mirror circuit; and

b. a common gate transistor.

26. The circuit of claim 25, wherein the third current mirror circuit further comprises a pair of same type MOS transistors.

27. The circuit of claim 15, wherein the output bias comprises at least one of (i) a PBias or (ii) an NBias.

28. A method for generating a periodic pulse signal for cell self refresh, comprising:

a. generating a leakage current from a memory cell;

b. transforming the leakage current into an output bias useful for determining a self refresh period; and

c. using the output bias to control an oscillator for generating a periodical signal pulse in response to the leakage current.

29. The method of claim 28, wherein generating a leakage currents from a memory cell further comprises:

a. generating a first leakage current of a "0" state cell; and

b. generating a second leakage current of a "1" state cell.

30. The method of claim 29, wherein generating a leakage currents from a memory cell further comprises generating third current.

31. The method of claim 29 further comprising connecting a storage node of the "0" state cell to a first current mirror circuit.

32. The method of claim 31 further comprising using the first current mirror circuit to generate a first current weighting factor.

33. The method of claim 29 further comprising connecting a storage node of the "1" state cell to a second current mirror circuit.

34. The method of claim 33 further comprising using the second current mirror circuit to generate a second current weighting factor.

35. A bias generator for cell self refresh for a semiconductor memory comprising a "0" state cell, capable of providing a first leakage current and a "1" state cell, capable of providing a second leakage current, where one of the first leakage current or second leakage currents dominates over the other of the first leakage current or second leakage currents, the bias generator comprising:

a. a current generator adapted to generate a third leakage current for a dominant leakage current from a memory cell; and

b. a converter coupled to the current generator, the converter adapted to transform the third leakage current into an output bias.